Amendment and Response
Applicant: Andrew H. Barr et al.
Serial No.: 10/714,302
Filed: Nov. 14, 2003
Docket No.: 200308580-1/H300.216.101
Title: SYSTEM AND METHOD FOR TESTING A MEMORY USING DMA

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of the claims:

1.   (Currently Amended) A computer system comprising:

a processor configured to execute an operating system;

a first bus coupled to the processor;

a memory; and

a core electronics complex including:

a memory controller coupled to the first bus and the memory;

a first input/output (I/O) controller coupled to the first bus and configured to couple to a first set of one or more I/O devices using a first connection; and

a test module coupled to the first I/O controller using a second connection that is separate from the first connection and the first bus;

wherein the test module is configured to provide test transactions to the first I/O controller using the second connection, and wherein the first I/O controller is configured to provide the test transactions to the memory controller using the first bus to cause tests to be performed on the memory using the first bus.

2.   (Currently Amended) The computer system of claim 1 further comprising:

an the operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using the first bus subsequent to the operating system being booted.

3.   (Currently Amended) The computer system of claim 1 further comprising:

an the operating system;

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wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using the first bus during execution of the operating system.

4.   (Original) The computer system of claim 1 wherein the first bus comprises a system bus.

5.   (Previously Presented) The computer system of claim 1 further comprising:
        a second bus; and
        a second set of one or more I/O devices coupled to the second bus;
        wherein the core electronics complex includes a second I/O controller coupled to the first bus and the second bus.

6.   (Previously Presented) The computer system of claim 1 wherein the test transactions include read and write transactions.

7.   (Original) The computer system of claim 6 wherein the read and write transactions comprise direct memory access (DMA) transactions.

8.   (Currently Amended) The computer system of claim 1 further comprising:
        a bus bridge coupled to the first bus and the first I/O controller; and
        wherein the first I/O controller is configured to provide the test transactions to the bus bridge, and wherein the bus bridge is configured to provide the test transactions to the memory controller using the first bus.

9.   (Currently Amended) A method performed by a computer system that includes a memory comprising:
        selecting a portion of the memory for testing during operation of the computer system;

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generating a test transaction in a test module coupled to an input/output (I/O) controller using a first connection that is separate from a second connection that is configured to couple the I/O controller to one or more I/O devices and separate from a system bus coupled to a processor, the test module and the I/O controller included in a chipset coupled to the memory and the system bus;

providing the test transaction from the test module to the I/O controller using the first connection;

providing the test transaction from the I/O controller to a memory controller; and

providing the test transaction from memory controller to the portion through the I/O controller using direct memory access (DMA).

10. (Original) The method of claim 9 further comprising:

detecting an error that occurs in response to the test transaction; and

performing a remedial action in response to detecting the error.

11. (Currently Amended) The method of claim 9 further comprising:

providing the test transaction from the test module to the I/O controller; providing the test transaction from the I/O controller to a bus bridge included in the chipset;

providing the test transaction from the bus bridge to a the system bus; and

providing the test transaction from the system bus to a the memory controller; and providing the test transaction from the memory controller to the portion.

12. (Original) The method of claim 11 further comprising:

storing information in the memory in response to the test transaction being a write transaction.

13. (Original) The method of claim 11 further comprising:

in response to the test transaction being a read transaction:

providing information associated with the test transaction from the portion to the memory controller;

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providing the information from the memory controller to the system bus;

providing the information from the system bus to the bus bridge;

providing the information from the bus bridge to the I/O controller; and

providing the information from the I/O controller to the test module.

14.   (Currently Amended) The method of claim 9 further comprising:

~~providing the test transaction from the test module to the I/O controller;~~

providing the test transaction from the I/O controller to a system controller included in the chipset; <u>and</u>

providing the test transaction from the system controller to ~~a~~ <u>the</u> memory controller~~;~~

~~and~~

~~providing the test transaction from the memory controller to the portion.~~

15.   (Currently Amended) A computer system comprising:

a processor<u> configured to execute an operating system</u>;

a bus coupled to the processor;

a memory;

a core electronics complex including:

    a system controller coupled to the bus and the memory;

    an input /output (I/O) controller coupled to the system controller and

configured to couple to a set of one or more I/O devices using a first connection; and

    a test module coupled to the I/O controller using a second connection that is

separate from the first connection<u> and the bus</u>;

wherein the test module is configured to provide test transactions to the I/O controller

<u>using the second connection, and wherein the I/O controller is configured to provide the test</u>

<u>transactions to the memory controller using the bus</u> to cause tests to be performed on the

memory using direct memory access (DMA).

16.   (Currently Amended) The computer system of claim 15 further comprising:

~~an~~ <u>the</u> operating system;

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wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using DMA subsequent to the operating system being booted.

17.   (Currently Amended) The computer system of claim 15 further comprising:

   an the operating system;

   wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using DMA during execution of the operating system.

18.   (Original) The computer system of claim 15 wherein the bus comprises a system bus.

19.   (Previously Presented) The computer system of claim 15 wherein the test transactions include read and write transactions.

20.   (Original) The computer system of claim 19 wherein the read and write transactions comprise direct memory access (DMA) transactions.